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10/706,457	11/12/2003	John G. Edelen	2003-0434.02	6755

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LEXMARK INTERNATIONAL, INC.
INTELLECTUAL PROPERTY LAW DEPARTMENT
740 WEST NEW CIRCLE ROAD
BLDG. 082-1
LEXINGTON, KY 40550-0999

EXAMINER	
NGUYEN, LAM S	
ART UNIT	**PAPER NUMBER**
2853	

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06/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/706,457	EDELEN ET AL.	
	Examiner	Art Unit	
	LAM S. NGUYEN	2853	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,13-20 and 23-28* is/are rejected.

7)☒ Claim(s) *9-12,21 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The Applicant's arguments filed in Appeal Brief dated 01/22/2007 regarding to claims 9-12 and 21-22 have been found persuasive. As a result, the finality is withdrawn.

Claim Objections

Claim 10 is objected to because of the following informalities: The claim recites "the semiconductor substrate" without sufficient antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-2, 4-8, 13-14, 16-20, 23-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa (US 6474782) in view of Lambertson (US 5544103).

Referring to claims 1, 13, 23:

Furukuwa disclose an ink jet printhead having a substrate (*FIG. 11, element H1100*) for a micro-fluid ejecting device, the substrate comprising:

a plurality of fluid ejection devices (*FIG. 11, elements HEATER ARRAY*);

a plurality of driver devices (*FIG. 11, elements DRIVER*) for driving the plurality of fluid ejection devices;

a nonvolatile memory (*column 13, lines 20-21*) being capable of being operatively

connected to the micro-fluid ejecting device for storing information for operation of the micro-fluid ejecting device (*column 13, lines 20-27: The information is heater resistance values, for example*) and directly readable by a controller (*Fig. 11, element 122*).

wherein the printhead is attached to a cartridge body having an ink supply source (*FIG. 4*), wherein the printhead is in fluid communication with the ink supply source and also has a nozzle plate (*FIG. 5, elements H1100 and H1100T*) attached to the substrate for ejecting ink therefrom upon activation of the ink ejection devices (**Referring to claim 13**).

Furukawa, however, is silent wherein the nonvolatile memory is a matrix containing embedded programmable memory devices embedded in a silicon semiconductor and comprises transistors selected from the group consisting of PMOS and NMOS floating gate transistors (**Referring to claims 2, 4, 14, 16, 26-28**), wherein the embedded programmable memory devices are programmable by applying a voltage of greater than about 8 volts for at least about 100 microseconds (**Referring to claims 6, 18**), wherein the memory matrix comprises more than 128 memory devices (**Referring to claims 5, 17**).

Lambertson discloses an integrated circuit nonvolatile memory matrix having more than 128 programmable memory devices (cells) (*column 1, lines 9-15 and column 39, lines 57-63*), embedded in a silicon semiconductor (*column 1, lines 17-18 and column 3, lines 64-68*), wherein each programmable memory device (cell) including transistors selected from the group consisting of PMOS and NMOS floating gate transistors (*FIG. 3 and column 18, lines 5-15*), wherein the embedded programmable memory devices are programmable by applying a voltage of greater than about 8 volts for at least about 100 microseconds (*column 18, lines 21-47: During*

programming process, the voltage on the floating gate is 7-10V; column 35, lines 40-45: The time programming is from 2-200 microseconds).

Therefore, it would have been obvious for one having ordinary skill in the art at the time invention was made to replace the nonvolatile memory in Furukuwa's printhead by Lambertson's nonvolatile memory comprising programmable memory device. The motivation for doing so would have been to allow erasing and programming the memory as taught by Lambertson (*Abstract*).

- **Referring to claims 7-8, 19-20:**

Furukuwa is also silent wherein the embedded programmable memory devices will pass from about 10 to about 200 microamps of current at about 2 volts in a programmed state and less than 3 microamps of current in an unprogrammed state.

Lambertson however also teaches that the memory device passes a current of 1-4mA under the voltage of 7-10V (*column 35, lines 62-67*) at the programmed state. Thus, at the voltage is about 2V, the current is about 0.3-0.8mA (300-800 microamps). During the unprogrammed state the current is less than 3 microamps (*column 35, lines 47-52: 0.5-5 nanoamps*).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to lower the current during the programmed state, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art.

2. Claims 3 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa (US 6474782) in view of Lambertson (US 5544103), as applied to claims 1 and 13, and further in view of Thakoor et al. (US 4876668).

Furukuwa, as modified, discloses the claimed invention as discussed above but is silent wherein the embedded programmable memory devices have a memory density of greater than about 200 bits per square millimeter.

Thakoor et al. discloses a programmable memory having a plurality of memory cells arranged in a density of greater than about 200 bits per square millimeter (*column 5, lines 63-68: Density of 10 bits/cm is the same as 10 bits/mm*).

Therefore, it would have been obvious for one having ordinary skill in the art at the time invention was made to modify the memory devices disclosed by Furukuwa, as modified, to having a density greater than 200 bits per square millimeter as disclosed by Thakoor et al. since it has been held as well known in the art that the higher density would reduce the packing size of the memory or increase the capacity of the memory.

Allowable Subject Matter

3. Claims 9, 11-12, and 21-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 10 would be allowable if rewritten to overcome the claim objection, set forth in this Office action.

Referring to claims 9 and 21-22: The primary reasons for the indication of the allowability of the claims is the inclusions therein, in combination as currently claimed, of the limitation that a layer disposed adjacent the programmable memory matrix and having properties

sufficient to block ultraviolet light having a wavelength below about 400 nanometers or a polyimide nozzle plate having properties sufficient to block ultraviolet light having a wavelength below about 400 nanometers is neither disclosed nor taught by the cited prior art of record, alone or in combination.

Claims 10-12 are allowed because they depend directly/indirectly on claim 9.

Response to Arguments

Applicant's arguments with respect to claims 1, 13, and 23 have been found not persuasive. In response to the Applicant's argument that there was no motivation to combine Furukawa and Lambertson references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, one of ordinary skill in the art would know that since Furukawa's memory storing information of heater resistances whose values and characteristics change by time, temperature, and other factors, so such information needs to be updated or programmed accordantly. As a result, it is reasonable to believe that one would look to Lambertson's programmable memory because information stored in Lambertson's memory can be updated or reprogrammed. Therefore, it is obvious that replacing Furukawa's memory by Lambertson's programmable memory would obtain such benefits.

In addition, the application argued that there was no description of erasing the Lambertson EEPROM device by exposing the device to ultraviolet light. This argument is over commensurate the scope of the claim since such limitation is not included in claims 1, 13, or 23.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LAM S. NGUYEN whose telephone number is (571)272-2151. The examiner can normally be reached on 7:00AM - 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, STEPHEN D. MEIER can be reached on (571)272-2149. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LAM SON NGUYEN